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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/990,862 | 11/13/2001 | Jung-Yu Hsieh | JCLA7288 | 2708 |

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| ART UNIT | PAPER NUMBER |
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| 2814 | |

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/990,862 | Applicant(s) HSIEH ET AL. |
|---|---|---|
| | Examiner Thao X Le | Art Unit 2814 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,3-8,10 and 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10 and 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
4) ☐ Interview Summary (PTO-413) Paper No(s) _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5768192 to Eitan.

Regarding to claim 1, Eitan teaches a structure of a flash memory in fig. 2 comprising: a first oxide layer 18 positioned on the substrate 12, a dielectric layer 20 having a high dielectric constant positioned on the first oxide layer 18, a second oxide layer 22 positioned on the dielectric layer 20 having the high dielectric constant, wherein the first oxide layer, the dielectric layer having the high dielectric constant and the second oxide layer together form a charge trapping layer, column 7 line 55-60, wherein a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide, a gate 24 located on the second oxide layer 22 of the charge trapping layer, and a source /drain 14/16 region located at two lateral sides of the substrate 12.

Although the prior art does not specially disclose the a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide, this feature is seen to be inherent teaching of that limitation, because silicon nitride layer 20 of Eitan has high dielectric constant than that of silicon oxide layer 18/22; thus, the band gap of

silicon nitride is approximately 5 eV, while the band gap of silicon oxide is approximately 9 eV.

3. Claims 7-8 and 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 5,596,214 to Endo

Regarding to claim 7, Endo teaches a structure of a flash memory in fig. 3 comprising: a first oxide layer 3, column 14 line 57, positioned on substrate 1, a dielectric layer 11 having a high dielectric constant, column 14 line 67, positioned on the first oxide layer 3, wherein the dielectric layer 11 having the high dielectric constant and the first oxide layer together form a charge trapping layer, column 15 line 40, and the dielectric layer having the high dielectric constant is a mixture of material selected from a group consisting of $TiO_2$, table1, a gate 5 positioned on the dielectric layer 11 having the high dielectric constant, and a source /drain 6/7 regions positioned at two lateral sides of the substrate 1.

Regarding to claims 8 and 10-11, Endo teaches a structure wherein a band gap of dielectric layer 11 having the high dielectric constant is larger than that of $SiO_2$, column 14 line 67, wherein high dielectric constant layer11 is a mixture of materials selected from a group comprising of $TiO_2$, table 1.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1, 3-6 are rejected under 35 U.S.C. 102(e) as being anticipated by JP Pub. No. 2001-007230 to Komori et al.

Regarding to claim 1, Komori teaches a structure of a flash memory in fig. 1 comprising: a first oxide layer 7a positioned on the substrate 1, a dielectric layer 7b having a high dielectric constant positioned on the first oxide layer 7a, a second oxide layer 7c positioned on the dielectric layer 7b having the high dielectric constant, wherein the first oxide layer, the dielectric layer having the high dielectric constant and the second oxide layer together form a charge trapping layer, wherein a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide, a gate 8 located on the second oxide layer 7c of the charge trapping layer, and a source /drain 4a/4b region located at two lateral sides of the substrate 1.

Although the prior art does not specially disclose the a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide, this feature is seen to be inherent teaching of that limitations, because silicon nitride or $Ta_2O_5$ layer 7c of Komori has high dielectric constant than that of silicon oxide layer 7a; thus, their band gap would be smaller than that of silicon oxide.

Regarding to claim 3-6, Komori teaches a structure of a flash memory wherein the dielectric layer 7b having the high dielectric constant is greater than 8, [0055], because of the inherent property of transition metal oxides, which has the dielectric constant approximately 30 or higher Komori teaches that the metallic oxide such as $Ta_2O_5$ (tantalum oxide) can be used for dielectric layer 7b [0055]

6. Claims 1, 7 and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 633554 to Yoshikawa

Regarding to claim 1, Yoshikawa teaches a structure of a flash memory in fig. 4 comprising: a first oxide layer 13, column 13 line 5, positioned on the substrate 1, a dielectric layer 4/14 having a high dielectric constant layer 14 made of SiN, column 13 line 7, positioned on the first oxide layer 13, a second oxide layer 15, column 13 line 8, positioned on the dielectric layer 4/14 having the high dielectric constant, wherein the first oxide layer, the dielectric layer 4/14 having the high dielectric constant layer 14 and the second oxide layer together form a charge trapping layer 4/14, wherein a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide, a gate 3 located on the second oxide layer 15 of the charge trapping layer 4/14, and a source /drain 10/11 region located at two lateral sides of the substrate 1.

Although the prior art does not specially disclose the a band gap of the dielectric layer having the high dielectric constant is smaller than that of silicon oxide, this feature is seen to be inherent teaching of that limitation, because silicon nitride layer 14 of Yoshikawa has high dielectric constant than that of silicon oxide layer 13/15; thus, the band gap of silicon nitride is approximately 5 eV, while the band gap of silicon oxide is approximately 9 eV.

Regarding to claim 7, Yoshikawa teaches a structure of a flash memory in fig. 4 comprising: a first oxide layer 13, column 13 line 5, positioned on substrate 1, a dielectric layer 4/14 having a high dielectric constant layer 14, column 18 line 14, positioned on the first oxide layer 13, wherein the dielectric layer 14 having the high dielectric constant and the first oxide

layer together form a charge trapping layer 4/14, and the dielectric layer 4/14 having the high dielectric constant layer 14 is a mixture of material selected from a group consisting of $TiO_2$, column 18 line 14, a gate 3 positioned on the dielectric layer 14 having the high dielectric constant, and a source /drain 10/11 regions positioned at two lateral sides of the substrate 1.

Regarding to claims 10-11, Yoshikawa teaches a structure wherein dielectric material 14 having the high dielectric constant is a mixture of materials selected from a group comprising of $TiO_2$, column 18 line 14.

***Response to Arguments***

7. Applicant's arguments with respect to claims 1, 3-8 and 10-11 have been considered but are moot in view of the new ground(s) of rejection. The Applicant argues that 'Yoshikawa does not anticipated the present invention because Yoshikawa teaches away from the present invention by having the charge trapping layers forming extensionally from the end of the of the gate electrode to a channel are direction. The arguments are not persuasive because claim in a pending application should be given their broadest reasonable interpretation. In re Pearson, 494F.ed 1399, 181 USPQ 641 (CCPA 1974). In this case, layers 4 and 14 are interpreted as 'a dielectric layer' as claimed.

***Conclusion***

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956

Thao X. Le
November 14, 2002